REMARKS

Claims 24, 25, 29 and 30, as amended, remain herein. Claims 26-28 and 31-34 remain herein but are presently withdrawn from consideration.

Claims 24 has been amended to clarify that the method comprises the single step of simultaneously and unitarily forming the wiring patterns and protrusions.

Claim 35, depending from claim 24, has been added, reciting modifying the protrusions to have substantially equal heights.

Claim 36, depending from claim 35, has been added, reciting wherein the modifying comprises imposing a load on the protrusions, see the paragraph bridging pages 13 and 14 of the specification.

Claim 29 has been amended to delete the phrase "the protrusions having substantially equal heights."

1. Claims 24 and 25 were rejected under 35 U.S.C. §102(b) over Abe U.S. Patent 5,746,868.

The presently claimed method of manufacturing a circuit board affirmatively recites simultaneously and unitarily forming the wiring patterns and the protrusions. This method is nowhere disclosed or suggested in the cited reference.

The Examiner alleges that Figs. 1A-E of Abe '868 describe simultaneously and unitarily forming element 9 with protrusions and wiring patterns. Applicants respectfully disagree. Abe '868, Fig. 1A, shows interconnection element 2 located on substrate 1, and column 5, lines 8-9, describes Fig. 1A as showing interconnection 2 "in a first layer" formed on substrate 1. Figs. 1B-C show intervening steps wherein insulating and protective films are formed on interconnection 2 to form surfaces in preparation for a future step of applying an additional metal conductor. Fig. 1D shows conductive paste 7 applied to hole 5 above interconnection 2. This step differs completely from step 1A and forms a layer different than the "first layer" formed in step 1A. And finally, Fig. 1E shows interconnection 9 formed on top of interconnection 2 after the paste is sintered and the protective film has been removed, as

described at column 5, beginning at line 65. Fig. 1E is separated from initial Step 1A by intervening steps shown in Figs. 1B-1D; while Fig. 1E shows a unitary formation of interconnections 2 and 9 as a unitized structure, Abe '868 does not describe the method step of simultaneously "and" unitarily forming interconnections 2 and 9 to form the structure shown in Fig. 1E, because interconnection 9 is not made unitary with interconnection 2 until almost the very end of the manufacturing sequence, i.e., at a sintering substep of the last step 1E. Therefore, contrary to the statement in the Office Action, Abe '868 does not disclose the step of simultaneously "and" unitarily forming wiring patterns and protrusions, because steps 1A and 1E are not simultaneous in time, as required by applicants' claims.

For the foregoing reasons, Abe '868 fails to disclose all elements of applicants' claimed invention, and therefore is not a proper basis for rejection under §102. Claim 25, which depends from claim 24, is allowable for the same reasons as

claim 24. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

2. Claims 29 and 30 were rejected under §103(a) over Abe '868.

Claim 29 recites the limitations discussed above with regard to claim 24, i.e., a method comprising simultaneously and unitarily forming the wiring patterns and the protrusions. This method is nowhere disclosed or suggested in the cited reference.

Contrary to the statement in the Office Action, Abe '868 does not disclose all of the limitations of claim 29, because Abe '868 does not disclose simultaneously and unitarily forming the wiring patterns and the protrusions, as discussed herein.

The Examiner admits that Abe '868 does not disclose coupling electrically the protrusion with a semiconductor chip component, and alleges that it is known in the art to electrically couple a protrusion with a chip component to form a motherboard. Nevertheless, such knowledge does not change the

fact that Abe '868 does not disclose all of the limitations of claim 29, as discussed herein.

For the foregoing reasons, Abe '868 does not contain any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicants' claimed invention. Claim 30, which depends from claim 29, is allowable for the same reasons as claim 29. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 24, 25, 29, 30, 35 and 36 are now proper in form and patentably distinguished over all grounds of rejection cited in the Office Action. Accordingly, allowance of all claims 24, 25, 29, 30, 35 and 36 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

If the only barrier to allowance is the presence of non-elected claims 26-28 and 31-34, the Examiner is authorized to cancel those claims without prejudice to applicants' rights to claim such subject matter in one or more divisional applications.

Respectfully submitted,

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